REMARKS/ARGUMENTS

Applicants have received the Office action dated August 19, 2005, in which the Examiner: 1) rejected claims 14-23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,347,337 ("Shah") in view of U.S. Pat. No. 6,044,406 ("Barkey"); 2) rejected claim 24 under 35 U.S.C. § 103(a) as being unpatentable over Shah, in view of Barkey and U.S. Pat. No. 6,674,722 ("Tiainen"); and 3) rejected claims 1-13 under 35 U.S.C. § 103(a) as being unpatentable over Shah in view of Barkey and further in view of U.S. Pat. No. 6,715,008 ("Shimizu") and U.S. Pat. No. 6,751,698 ("Deneroff").

With this Response, Applicants have amended claims 1, 7, 14, and 21. Also, Applicants canceled claims 8 and 15. Claims 1-7, 9-14 and 16-24 are pending. Based on the amendments and arguments presented herein, Applicants respectfully request reconsideration and allowance of the pending claims.

I. CLAIM REJECTIONS

Amended claim 1, in part, requires "the interprocessor router receives more credits than the cache control unit." Claim 1 further requires "memory requests from a local processor are delivered to the memory controller by [a] cache control unit" and "memory requests from other processors are delivered to the memory controller by the interprocessor router."

Applicants submit that claim 1 is allowable for at least two reasons. First, none of the references cited by the Examiner, nor combinations of the references, teach or suggest "[an] interprocessor router receives more credits than [a] cache control unit" as required in claim 1.

Second, the Examiner recognizes that neither Shah nor Barkey teach Applicants' claimed "memory requests from a local processor are delivered to the memory controller by [a] cache control unit" and "memory requests from other processors are delivered to the memory controller by the interprocessor router" as required in claim 1. Instead, the Examiner suggests Shimizu teaches "memory requests from other processors are delivered to the memory controller by the

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interprocessor router" and Deneroff teaches "memory requests from a local processor are delivered to the memory controller by [a] cache control unit."

Applicants cannot find where Shimizu teaches "memory requests from other processors are delivered to the memory controller by the interprocessor router" and where Deneroff teaches "memory requests from a local processor are delivered to the memory controller by the cache control unit" as required in claim 1. For example, Deneroff mentions that a memory controller could optionally include a directory controller that provides cache coherence (see col. 2, lines 32-40), but does not appear to specifically teach or suggest "memory requests from a local processor are delivered to the memory controller by [a] cache control unit" as required in claim 1.

If the Examiner believes the above limitations are inherent to the cited references, the Examiner has not provided rationale or evidence tending to show inherency as is required (see MPEP 2112). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534. For at least these reasons, Applicants submit that claim 1 is allowable.

Amended claim 7, in part, requires "if a source has no available credits, the source does not send request or response commands to the request buffer and wherein if the source has one available credit, the source reserves the one available credit to send a response command to the request buffer." While the Examiner appears to address the limitation "if a source has no available credits, the source does not send request or response commands to the request buffer," the Examiner does not appear to address the limitation "if the source has one available credit, the source reserves the one available credit to send a response command to the request buffer." None of the references cited by the Examiner, nor combinations of the references, appear to teach or suggest "if the source has one available credit, the source reserves the one available credit to send a response command to the request buffer" as required in claim 7. For at least these reasons, Applicants submit that claim 7 and all claims that depend from claim 7 are allowable.

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Amended claim 14, in part, requires "assigning credits to each of a plurality of sources that sends data packets to the shared buffer." Claim 14 further requires "when the number of empty buffer spaces is smaller than the buffer threshold and a buffer space becomes empty, automatically returning a credit in a random manner to one of the sources that have spent credits held by the buffer."

The Examiner suggests that Shah teaches Applicants' claimed "when the number of empty buffer spaces is smaller than the buffer threshold and a buffer space becomes empty, automatically returning a credit in a random manner to one of the sources that have spent credits held by the buffer" (see Office Action, page 3, item 5). Applicants disagree for at least two reasons. First, Shah does not appear to teach returning credits to one of "a plurality of sources" as required in claim 14. For example, the citation provided by the Examiner (Shah, col. 2, lines 36-41) mentions credits and a threshold value, but does not mention "a plurality of sources" are involved as required in claim 14. Second, even if Shah was interpreted as applying to a plurality of sources, Shah still does not teach or suggest "returning a credit in a random manner to one of the sources" as required in claim 14. None of the references cited by the Examiner, nor combinations of the references, appear to teach or suggest this limitation. For at least these reasons, Applicants submit that claim 14 and all claims that depend from claim 14 are allowable.

Amended claim 21, in part, requires "a first source and a second source." Claim 21 further requires that "the first source receives more credits than the second source." None of the references cited by the Examiner, nor combinations of the references, appear to teach or suggest "[a] first source receives more credits than [a] second source" as required in claim 21. As stated in MPEP 2112, "the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." *In re Rijckaert*, 9 F.3d 1531, 1534. For at least these reasons, Applicants submit that claim 21 and all claims that depend from claim 21 are allowable.

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II.   CONCLUSIONS

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

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